YHM4207

Single Channel Bi-direction Voltage-Level Translator

Features

- Single 1.6V to 5.5V Supply Voltage
- Enable and High Voltage Supply from VCCEN
- Low Voltage Decided by Internal LDO, down to 0.9V
- Supports 10MHz Open-Drain Operation without external pull up resistor
- Low Transmission Gate Ron: 20Ω
- Pullup Resistor Enabled for High Voltage Side
- 1.3uA Supply Current
- 2.07mm x 2.30mm 6-pin SC70

Applications

- UART, GPIO, and other signal interfaces

General Description

The YHM4207 is a single channel, bidirectional UART or GPIO voltage-level translator, designed specifically for low power consumption making it suitable for portable and battery powered equipment. Externally applied voltages VH and VL, set the logic levels on either side of the device. A logic signal present on the VL side of the device appears as the same logic signal on the VH side of the device, and vice-versa.

The device is operational from 0.9V to 3.3V VL and 1.6V to 5.5V VH, with only one VCCEN pin which is tied to VH for enable and internal LDO input. The VL is decided by internal LDO output, which can be used for 0.9V/1.2V/1.8V/2.5V/3V/3.3V system IO by different device version A/B/C/D/E. When VCCEN is low, the translator switch is off, and a high-impedance state exists between ports.

The Device also integrate one shot block to reduce the rise time for high speed application.

The YHM4207 comes in a 6 PIN, 2.07mm x 2.30mm SC70-6 package.

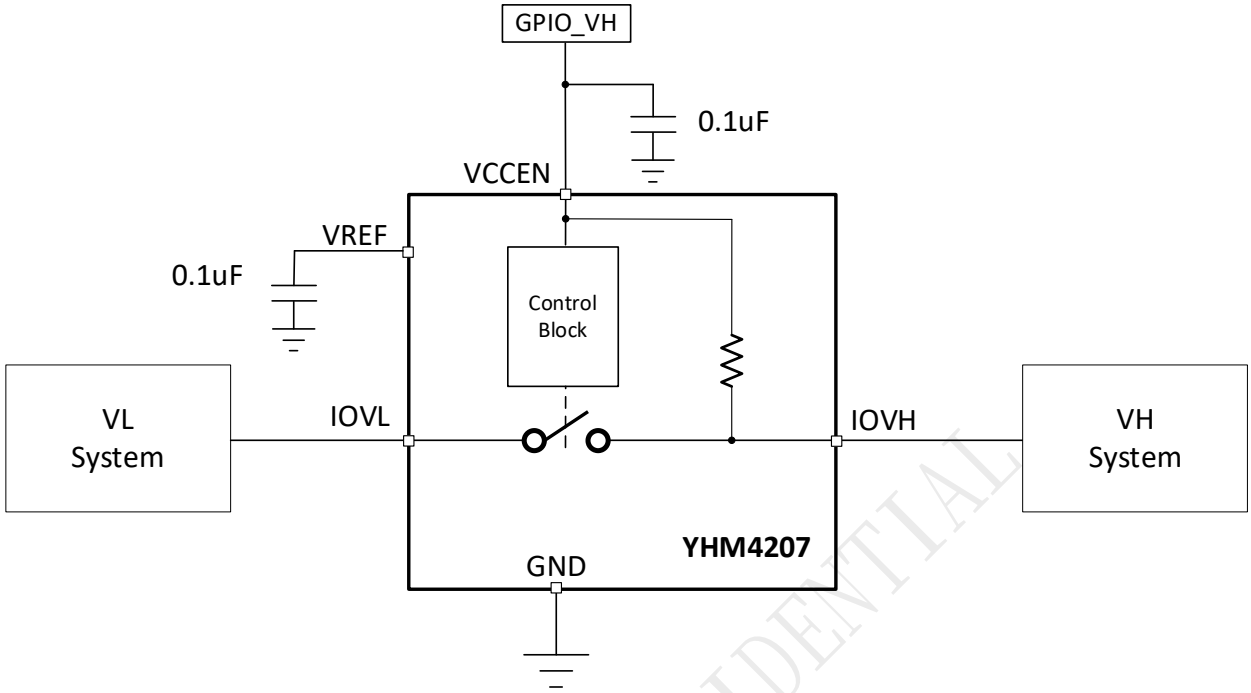


Fig 1. YHM4207 Internal Block Diagram

YHM4207 Pin Configurations

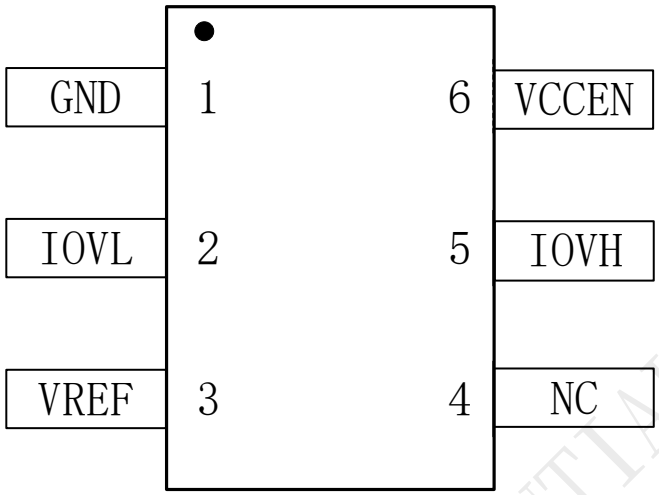


Fig 2. YHM4207 SC70-6 Pin Assignment(Top Through View）

YHM4207 SC70 Pin Descriptions

SC70	Name	Description
1	GND	Ground.
2	IOVL	Low Voltage Input/Output. Reference to VL.
3	VREF	Connect a 0.1uF capacitor to ground.
4	NC	Not Connected.
5	IOVH	High Voltage Input/Output. Reference to VH.
6	VCCEN	Power Supply and Enable. Connect to VH GPIO. Bypass a 0.1uF capacitor.

1 Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Disclaimer: YHMICROS reserves the right to make any change in circuit design, specification or other related things if needed without notice at any time.

Symbol	Parameters		Min.	Max.	Unit
VCCEN	VCCEN to GND		-0.3	6	V
V_{IOVH}	IOVH to GND		-0.3	6	V
V_{REF}	VREF to GND		-0.3	6	V
V_{IOVL}	IOVL to GND		-0.3	6	V
I_{VCCEN}	Continuous Input Current			100	mA
I_{IO}	Continuous channel current			±100	mA
t_{PD}	Total Power Dissipation at T_A=25°C				mW
T_{STG}	Storage Junction Temperature		-65	+150	°C
T_J	Operating Junction Temperature			+150	°C
T_L	Lead Temperature (Soldering, 10 Seconds)			+260	°C
θ_{JA}	Thermal Resistance, Junction-to-Ambient (100mm^2 pad of 1 oz. copper)				°C/W
All Pins	Electrostatic Discharge Capability	Human Body Model, EIA/JESD22-A114	2		KV
		Charged Device Model, JESD22-C101	1		

Note 1. Refer to JEDEC JESD51-7, use a 4-layerboard

2 Detailed Electrical Characteristics

(VCCEN = 1.8V, T_A = -40°C to +85°C. Typical values are at T_A = +25°C, unless otherwise noted T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
Supply Voltage Range	VCCEN		1.6		5.5	V
Quiescent Supply Current	I_{VCCEN}	T_A =+25°C		1.3		μA
		-40°C ≤ T_A ≤ +85°C			4	
IOVL, IOVH Three-State Leakage Current	I_{LEAK}	VCCEN = GND, V_I = 1.2V			1	uA
VCCEN Shutdown Threshold	V_{TH}	VCCEN failing		0.7		V
IOVL to IOVH Resistance	R_{ON}	VCCEN = 1.8V, V_I = 0V, I_O = 15mA		8		Ω
IOVH Pull Up Resistor	R_{IOV}			5		kΩ
High Side Voltage	VH	VH=VCCEN	1.6		5.5	V
Low Side Voltage without pull up resistor	VL'	YHM4207A, for 0.9V VL VCCEN=VH=3.3V		0.81		V
		YHM4207B, for 1.2V VL VCCEN=VH=3.3V		1.08		
		YHM4207C, for 1.8V VL VCCEN=VH=3.3V		1.62		
		YHM4207D, for 2.5V VL VCCEN=VH=3.3V		2.25		
		YHM4207E, for 3V and 3.3V VL VCCEN=VH=3.6V		2.97		
AC SPECIFICATIONS (C_{IOVH} ≤ 50pF, C_{IOVL} ≤ 50pF. All timing is 10% to 90% for rise time and 90% to 10% for fall time).						
Turn On Time	t_{ON}	VCCEN from 0 to 1.8V		50		μs
IOVL Rise Time	t_{RH}	Open-drain driving, VL = 1.2V, VH = 1.8V		50		ns
IOVL Fall Time	t_{FH}	Open-drain driving, VL = 1.2V, VH = 1.8V		45		ns
IOVH Rise Time	t_{RH}	Open-drain driving, VL = 1.2V, VH = 1.8V		125		ns
IOVH Fall Time	t_{FH}	Open-drain driving, VL = 1.2V, VH = 1.8V		50		ns
Maximum Data Rate		Open-drain operation		10		MHz
THERMAL PROTECTION						
Thermal Shutdown	T_{SHDN}			150		ºC
Thermal Hysteresis	T_{HYST}			20		ºC

Note 1: All specifications are 100% production tested at T_A = +25°C, unless otherwise noted. Specifications are over T_A = -40°C to +85°C and are guaranteed by design.

Note 2: Guaranteed by design; not production test.

3 Detailed Description

3.1 General Introduction

The YHM4207 is a single channel, bidirectional level translator. The device translates low voltage down to +1.2V on the VL side to high voltage on the VH side and vice-versa. The device has low on-resistance (20Ω max), which is important for high speed, open-drain operation. The device also features an internal 10KΩ pullup resistor for VH side when VCCEN is high.

3.2 Level Translation

For proper operation, connect VCCEN to VH power, ensure that +1.6V ⩽ VH ⩽ +5.5V, +0.9V ⩽ VL ⩽ VH and choose the right A/B/C/D/E device version for 0.9V/1.2V/1.8V/2.5V/3V/3.3V IO for different application. The device integrates an adjustable LDO to generate a 0.9*VL+V_{TH} voltage to control translation FET, while V_{TH} is a threshold voltage around 0.6V.

The device features a three-state input that can put the device into high-impedance mode. When VCCEN is low, IOVH and IOVL are all high impedance and the internal pullup resistor is disconnected. When VCCEN is high, the internal pullup resistor is connected. With this feature, the device can also support push pull bidirectional voltage translation without direction control.

3.3 High-Speed Operation

The YHM4207 have an internal one shot block as rise time accelerator, allowing operation up to 10MHz. The accelerator is present on VH side of the device and act to speed up the rise time of VL side to VH side. The triggering mechanism is when V_{IOVH} reach 0.7*VL, internal pull up to VH shortly. To guarantee operation of the rise time accelerators the maximum parasitic capacitance should be less than 200pF on the I/O lines.

3.4 System Design

As Figure 1 shows, VCCEN should be connected to high voltage side VH. A 100pF filter capacitor connected to VCCEN is recommended. As with the standard I2C system, pullup resistors are required to provide the logic-high levels on the translator bus. The size of these pullup resistors depends on the system. The internal 10KΩ on VH side need to be taken into consideration.

In I2C applications, the bus capacitance limit of 400pF restricts the number of devices and bus length. The capacitive load on both sides of the device must be taken into account when approximating the total load of the system, ensuring the sum of both sides is under 400pF. Both channels of the device have the same electrical characteristics, and there is minimal deviation from one output to another in voltage or propagation delay. This is a benefit over discrete transistor voltage-translation solutions, because the fabrication of the switch is symmetrical. The translator provides excellent ESD protection to lower-voltage devices and at the same time protects less-ESD-resistant devices.

4 Parameter Measurement Information

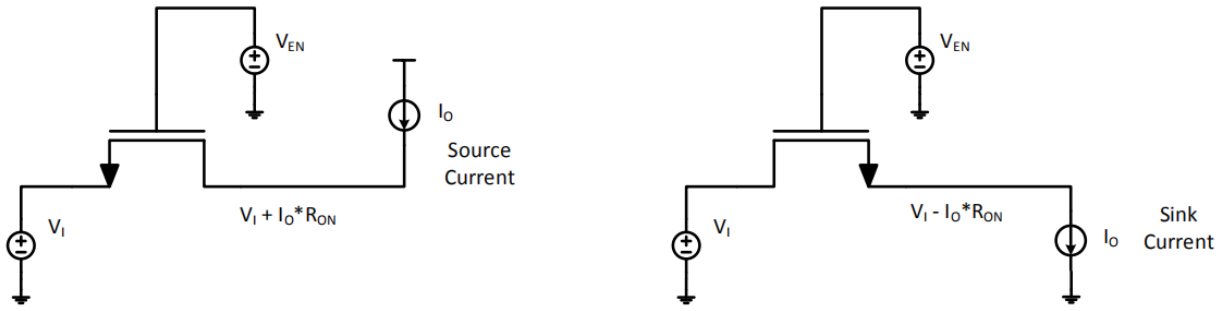
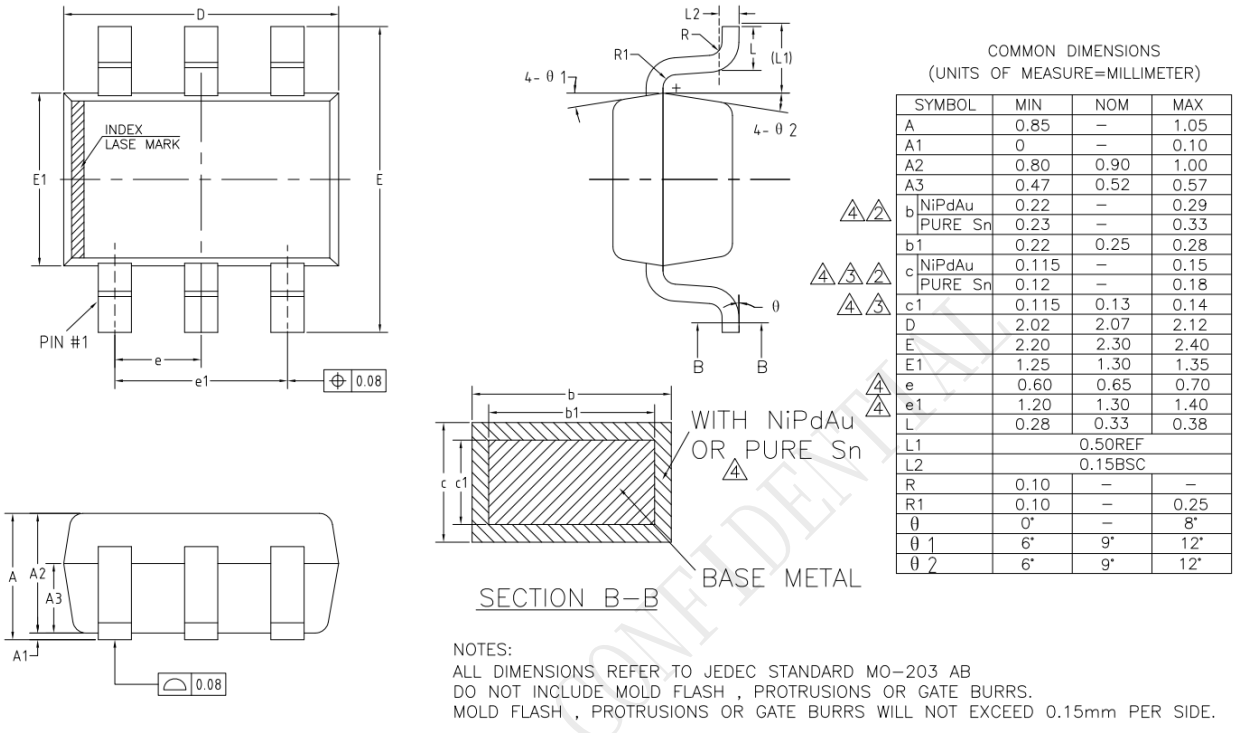


Fig 3. Current Source and Current Sink Configurations for R_{ON} Measurements

Package Dimensions

SC70-6 2.07 x 2.30 x 0.95



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL		MIN	NOM	MAX
A		0.85	–	1.05
A1		0	–	0.10
A2		0.80	0.90	1.00
A3		0.47	0.52	0.57
4 2 b	NiPdAu	0.22	–	0.29
	PURE Sn	0.23	–	0.33
b1		0.22	0.25	0.28
4 3 2 c	NiPdAu	0.115	–	0.15
	PURE Sn	0.12	–	0.18
4 3 c1		0.115	0.13	0.14
D		2.02	2.07	2.12
E		2.20	2.30	2.40
E1		1.25	1.30	1.35
4 e		0.60	0.65	0.70
4 e1		1.20	1.30	1.40
L		0.28	0.33	0.38
L1		0.50REF		
L2		0.15BSC		
R		0.10	–	–
R1		0.10	–	0.25
θ		0°	–	8°
θ 1		6°	9°	12°
θ 2		6°	9°	12°

NOTES:
ALL DIMENSIONS REFER TO JEDEC STANDARD MO-203 AB
DO NOT INCLUDE MOLD FLASH , PROTRUSIONS OR GATE BURRS.
MOLD FLASH , PROTRUSIONS OR GATE BURRS WILL NOT EXCEED 0.15mm PER SIDE.

Ordering Information

Part Number	Temp Range	Pin Package	Top Mark	MOQ
YHM4207AS6T	-40°C to 85°C	6 SC70	XXX5A	3000
YHM4207BS6T	-40°C to 85°C	6 SC70	XXX5B	3000
YHM4207CS6T	-40°C to 85°C	6 SC70	XXX5C	3000
YHM4207DS6T	-40°C to 85°C	6 SC70	XXX5D	3000
YHM4207ES6T	-40°C to 85°C	6 SC70	XXX5E	3000

T = Tape and reel.
XXX = The last three number of LOTID.

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