YHM1107A/B/C

High Voltage Low Ron DPST Switch with OVP

Features

- VCCEN voltage range: 1.1V ~ 5.5V
- COM/NO recommend voltage range: -3V~16V
- COMx to NOx On-resistance: typical 110mΩ each
- Max 1.5A continuous current capability each
- Peak 2.5A current (<1ms) capability each
  YHM1107A: 3.6V OVP (in NO1/2)
  YHM1107B: 5.8V OVP (in NO1/2)
  YHM1107C: 9.6V OVP (in NO1/2)
- -106dB THD
- -96dB Off Isolation and -88dB Cross talk
- OTP (Over Temperature Protection)
- Robust ESD capability:
  ±2kV HBM, ±1kV CDM

Applications

- Smart Phone, AR/VR Device, Tablet PC, Wearable etc.

General Description

The YHM1107 family are high voltage low Ron dual pole single throw and bidirectional on/off switches with Max 18V tolerance in COM1/2 and NO1/2 PIN.

The YHM1107 family combine enable and supply pin. The switch is on when device is powered. Connect VCCEN to GND to turn-off the switch. The topology of the switch allows the signal over VCCEN without the need of an external discrete components.

The YHM1107 family have excellent on-resistance matching (2mΩ Typical) between SPST switch and on-resistance flatness over whole signal range. These ensure perfect linearity and very low distortion for audio signal through.

YHM1107 does not have OVP function. YHM1107A supports 3.6V OVP in NO1/2. YHM1107B supports 5.8V OVP in NO1/2. YHM1107C supports 9.6V OVP in NO1/2. YHM1107A/B/C may do UART, CC, audio jack or other digital/analog interface protector.

The YHM1107 family come in a 2x3 array, 6-bump, 0.4mm pitch, 0.815mmx1.17mm wafer-level package (WLP).

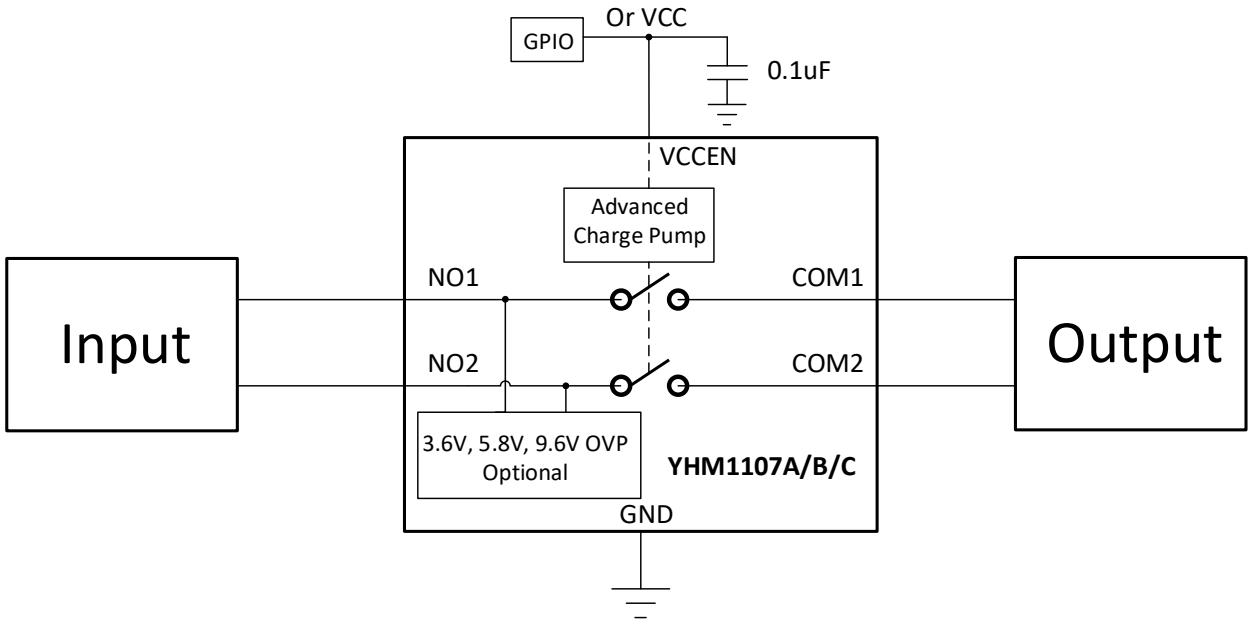


Fig 1. YHM1107 Internal Block and System Diagram

YHM1107 Pin Configurations

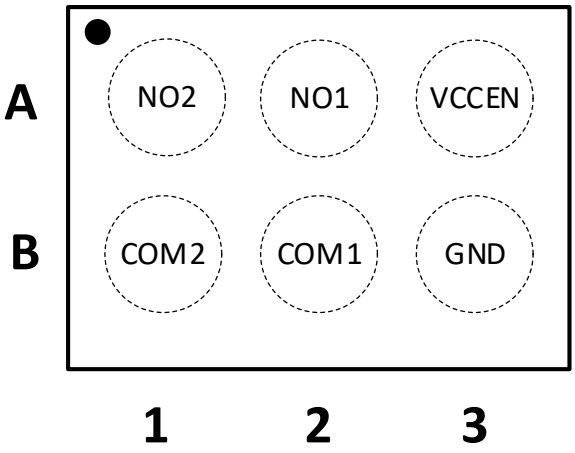


Fig 2. YHM1107 WLP-6 Pin Assignment(Top Through View）

YHM1107 WLP Pin Descriptions

WLP	Name	Description
A1	NO2	Normally Open Terminal for SPST Switch 2
A2	NO1	Normally Open Terminal for SPST Switch 1
A3	VCCEN	Supply Voltage Enable Input, bypass VCCEN to GND with 0.1uF capacitor as close to the chip as possible
B1	COM2	Common Terminal for SPST Switch 2
B2	COM1	Common Terminal for SPST Switch 1
B3	GND	Ground

Function Table

VCCEN	SPST SWITCH 1	SPST SWITCH 2
0	COM1 TO NO1 SWITCH OFF	COM2 TO NO2 SWITCH OFF
1	COM1 TO NO1 SWITCH ON	COM2 TO NO2 SWITCH ON

1 Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameters		Min.	Max.	Unit
VCCEN	VCCEN to GND		-0.3	6	V
$V_{COM1/2}$, $V_{NO1/2}$	Voltage of COM1/2 and NO1/2 to GND		-5	18	V
I_{IN}	SPST Switch I/O Current (Continuous) each path			±1.5	A
I_{IN_PEAK}	SPST Switch I/O Current (Peak, <1ms) each path			±2.5	A
t_{PD}	Total Power Dissipation at T_A=25°C				
T_{STG}	Storage Junction Temperature		-65	+150	°C
T_J	Operating Junction Temperature			+150	°C
T_L	Lead Temperature (Soldering, 10 Seconds)			+260	°C
θ_{JA}	Thermal Resistance, Junction-to-Ambient (100mm^2 pad of 1 oz. copper)				
All Pin	Electrostatic Discharge Capability	Human Body Model, EIA/JESD22-A114	2		KV
		Charged Device Model, JESD22-C101	1		

Note 1. Refer to JEDEC JESD51-7, use a 4-layerboard

2 Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance.

Parameters	Min.	Max.	Unit
Supply Voltage to Enable the Chip: VCCEN	1.1	5.5	V
Signal Swing Range through SPST Switch: COM1/2, NO1/2	-3	16	V
SPST Switch I/O Current (Continuous) each path: I_{IN}		1.5	A
SPST Switch I/O Current (Peak, <1ms) each path: I_{IN_PEAK}		2.5	A
Ambient Operating Temperature, T_A	-40	85	°C
VCCEN Capacitor	0.1		μF

3 Detailed Electrical Characteristics

(Unless otherwise noted, VCCEN =1.1V to 5.5V, T_A = -40°C to 85°C; Typical values are at VCCEN = 2.5V, C_{VCCEN} = 0.1μF and T_A = 25ºC.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
Power-Supply Range	VCCEN		1.1		5.5	V
Power-Supply Rejection Ratio	PSRR	R_{COM} = 32Ω, f = 20kHz		96		dB
Supply Current	I_{CC}	VCCEN = 1.2V		55		μA
		VCCEN = 1.8V		42		
	I_{OFF}	VCCEN = 0V, V_{NO} or V_{COM}=2.5V		1		nA
ANALOG SWITCH						
Analog Signal Range	$V_{NO1/2}$, $V_{COM1/2}$		-3		+16	V
On-Resistance	R_{ON}	VCCEN = 2.5V, $V_{COM1/2}$ = 0V, $I_{COM1/2}$ = 100mA (Note 2)		110	150	mΩ
		VCCEN = 1.8V, $V_{COM1/2}$ = 0V, $I_{COM1/2}$ = 100mA (Note 2)		110	150	
On-Resistance Match Between Channels	Δ R_{ON}	VCCEN = 2.5V, $I_{COM1/2}$ = 100mA, between two channels		2		mΩ
On-Resistance Flatness	R_{FLAT}	VCCEN = 2.5V, $I_{COM1/2}$ = 100mA, $V_{COM1/2}$ = -0.3V to +16V (Note 3, Note 4)		0.1		mΩ
NO1/2, COM1/2 Off-Leakage Current	$I_{NO1/2}$(OFF), $I_{COM1/2}$(OFF)	VCCEN = 0V, $V_{NO1/2}$ = 16V, $V_{COM1/2}$ = 16V, unconnected		0.1		uA
		VCCEN = 0V, $V_{NO1/2}$ = 2.5V, $V_{COM1/2}$ = 2.5V, unconnected		10		nA
NO1/2, COM1/2 On-Leakage Current	$I_{NO1/2}$(ON), $I_{COM1/2}$(ON)	VCCEN = 2.5V, switch closed, $V_{COM1/2}$ = $V_{NO1/2}$ = 16V		1		uA
		VCCEN = 2.5V, switch closed, $V_{COM1/2}$ = $V_{NO1/2}$ = 2.5V		100		nA
NO1/2 Over-Voltage Trip Level	$V_{NO1/2\_OVLO}$	$V_{NO1/2}$ Rising, YHM1107A		3.6		V
		$V_{NO1/2}$ Rising, YHM1107B		5.8		
		$V_{NO1/2}$ Rising, YHM1107C		9.6		
OVLO Hysteresis	V_{HYS_OVLO}	YHM1107A/B/C		2		%
DYNAMIC TIMING						
Turn-On Time	t_{ON}	VCCEN from 0V to 2.5V, $V_{NO1/2}$ = 5.5V, R_L = 50Ω		770		us
Turn-Off Time	t_{OFF}	VCCEN from 2.5V to 0V, $V_{NO1/2}$ = 5.5V, R_L = 50Ω		5		us
OVP Response Time on NO1/2	t_{OVP}	R_L = 50Ω, time from $V_{NO1/2}$ > $V_{NO1/2\_OVLO}$ to $V_{COM1/2}$ = 0.1 × $V_{NO1/2}$		200		ns

AUDIO PERFORMANCE				
Total Harmonic Distortion Plus Noise	THD + N	f = 20Hz to 20kHz, V_{ON}= 1V_{P-P}, R_S=20Ω, R_L=32Ω	-105	dB
		f = 20Hz to 20kHz, V_{ON} = 1V_{P-P}, R_S=20Ω, R_L=8Ω	-102	
		f = 20Hz to 20kHz, V_{ON} = 1V_{RMS}, R_S=20Ω, R_L=32Ω	-98	
		f = 20Hz to 20kHz, V_{ON} = 1V_{RMS}, R_S=20Ω, R_L=8Ω	-102	
Off-Isolation	V_{ISO}	R_S = R_L = 50Ω; $V_{COM1/2}$ = 0.5V_{P-P}, f =1kHz, VCCEN = 0V, DC bias = 0.25V	-88	dB
Crosstalk	V_{CT}	R_S = R_L = 50Ω; $V_{COM1/2}$ = 0.5V_{P-P}, f = 1kHz	-96	dB
-3dB Bandwidth	BW	R_S = R_L = 50Ω	235	MHz
NO1/2 Off-Capacitance	$C_{NO1/2}$(OFF)	$V_{NO1/2}$ = 0.5V_{P-P}, f = 1MHz, COM1/2 unconnected	32	pF
COM1/2 On-Capacitance	$C_{COM1/2}$(ON)	$V_{NO1/2}$ = 0.5V_{P-P}, f = 1MHz	35	pF
THERMAL PROTECTION				
Thermal Shutdown	T_{SHDN}		140	ºC
Thermal Hysteresis	T_{HYST}		30	ºC

Note 1: All specifications are 100% production tested at T_A = +25°C, unless otherwise noted. Specifications are over T_A = -40°C to +85°C and are guaranteed by design.

Note 2: The same limits apply for $V_{COM1/2}$= -3V to +16V and are guaranteed by design.

Note 3: Flatness is defined as the difference between the maximum and minimum value of on-resistance, as measured over specified analog signal ranges.

Note 4: Guaranteed by design.

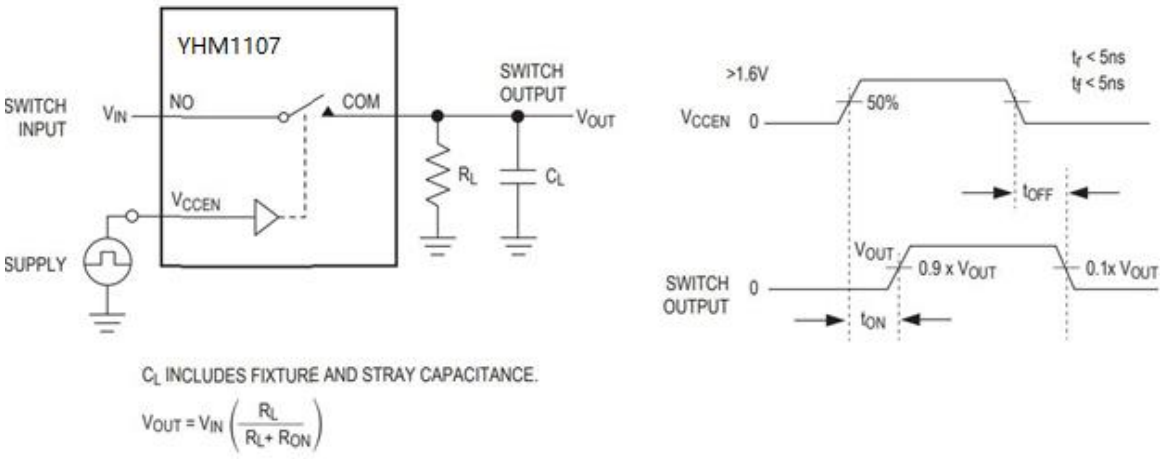


Fig 3. Test Circuit for Switching Times (t_{ON}, t_{OFF})

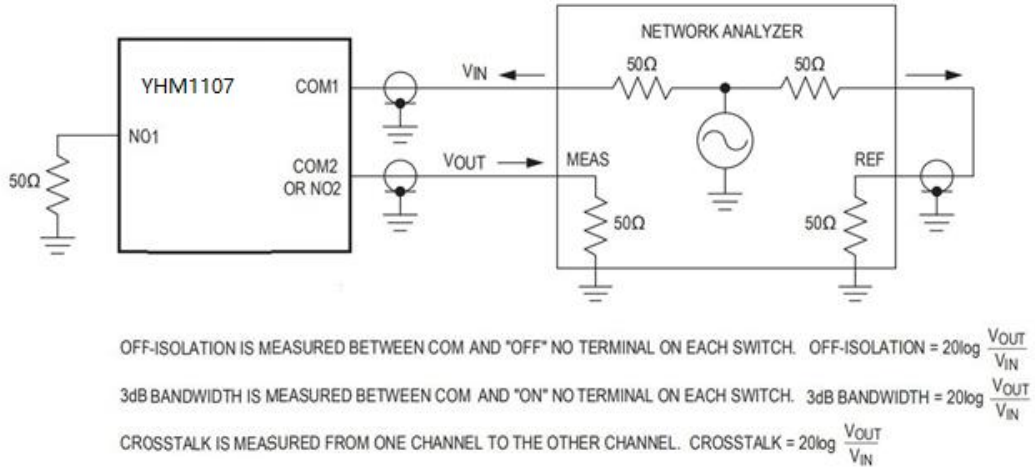


Fig 4. Test Circuit for OFF-ISOLATION, BANDWIDTH and CROSSTALK

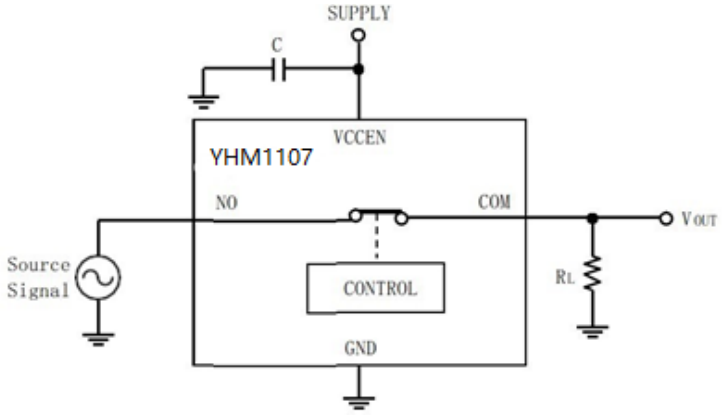


Fig 5. Test Circuit for Total Harmonic Distortion (THD)

Fig 6. Bandwidth 235MHz

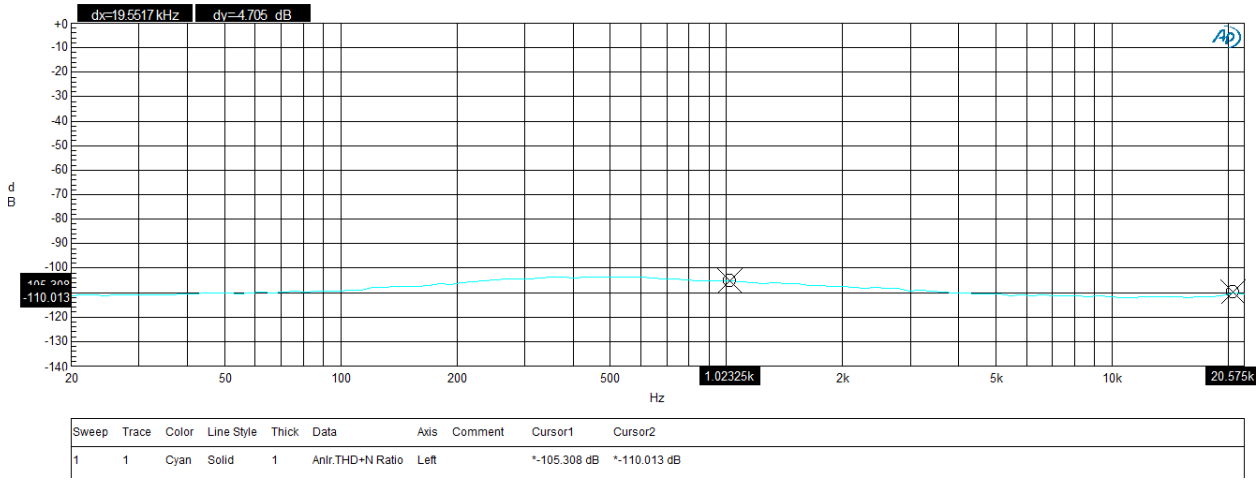


Fig 7. THD+N Performance with 105dB for $1V_{P-P}$ into 32Ω

4 Detailed Description

4.1 General Introduction

The YHM1107 family are ultra-small, low on-resistance, high ESD protected DPST switches that operate from a +1.1V to +5.5V supply, pass up to 16V analog or PWM signals, such as smart audio, video or control signals. The switch features the low on-resistance (RON) necessary for high-performance switching applications. The Beyond-the-Rails signal capability of the YHM1107 family allow signals below or above VCCEN to pass without distortion.

4.2 Analog Switch

The YHM1107 family are bidirectional, allowing NO1/2 and COM1/2 to be configured as either inputs or outputs. The topology of the switch allows the signal over VCCEN without the need of an external discrete components.

The YHM1107 family combine enable and supply pins. The switch is on when device is powered. Connect VCCEN to GND to turn-off the switch.

4.3 Over Voltage Lockout

The YHM1107A/B/C integrate Over Voltage Lockout function. Analog switch will be turned off whenever NO1/2 voltage higher than $V_{NO1/2\_OVLO}$. The value of $V_{NO1/2\_OVLO}$ is 3.6V for YHM1107A, 5.8V for YHM1107B and 9.6V for YHM1107C.

4.4 System design

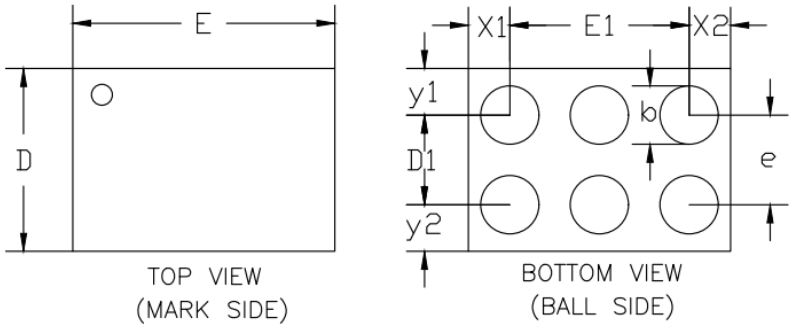
When the YHM1107 is on, to protect the chips from over temperature, the switch will be turned off when the junction temperature exceeds TSND = 140°C. The switch will be turned on again when temperature drop below 120°C. The device power dissipation capability is dependent on board design and layout. Mounting pad configuration on the PCB, the board material and the ambient temperature affect the rate of junction temperature rise for the part. When YHM1107 has good thermal conductivity through the PCB, the junction temperature will be relatively low under high power through applications. The maximum dissipation the YHM1107 can handle is given by:

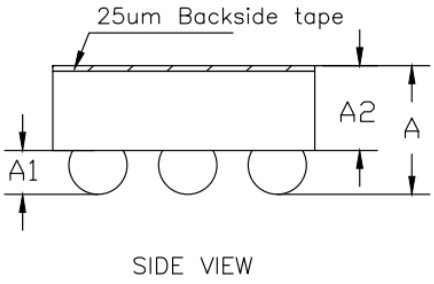
$$P_{D(MAX)}=[T_{J(MAX)}-T_A]/\theta_{JA}$$

A ceramic about 0.1uF capacitor is recommended and should be connected close to the YHM1107 VCCEN. Higher capacitance and lower ESR will improve the overall performance.

Package Dimensions

WLCSP-6 0.815x1.17x0.574





COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.534	0.574	0.614
A1	0.176	0.196	0.216
A2	0.358	0.378	0.398
D	0.795	0.815	0.835
D1	0.400BSC		
E	1.150	1.170	1.190
E1	0.800BSC		
b	0.240	0.260	0.280
e	0.400BSC		
x1	0.185 REF		
x2	0.185 REF		
y1	0.208 REF		
y2	0.208 REF		

Ordering Information

Part Number	Temp Range	Pin Package	Top Mark	MOQ
YHM1107AW6T	-40°C to 85°C	6 WLCSP	YWW LOT	3000
YHM1107BW6T	-40°C to 85°C	6 WLCSP	YWW LOT	3000
YHM1107CW6T	-40°C to 85°C	6 WLCSP	YWW LOT	3000

T = Tape and reel.
YWW: Date Code. Y = year, WW = week.
LOT: The last three number of LOTID.

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